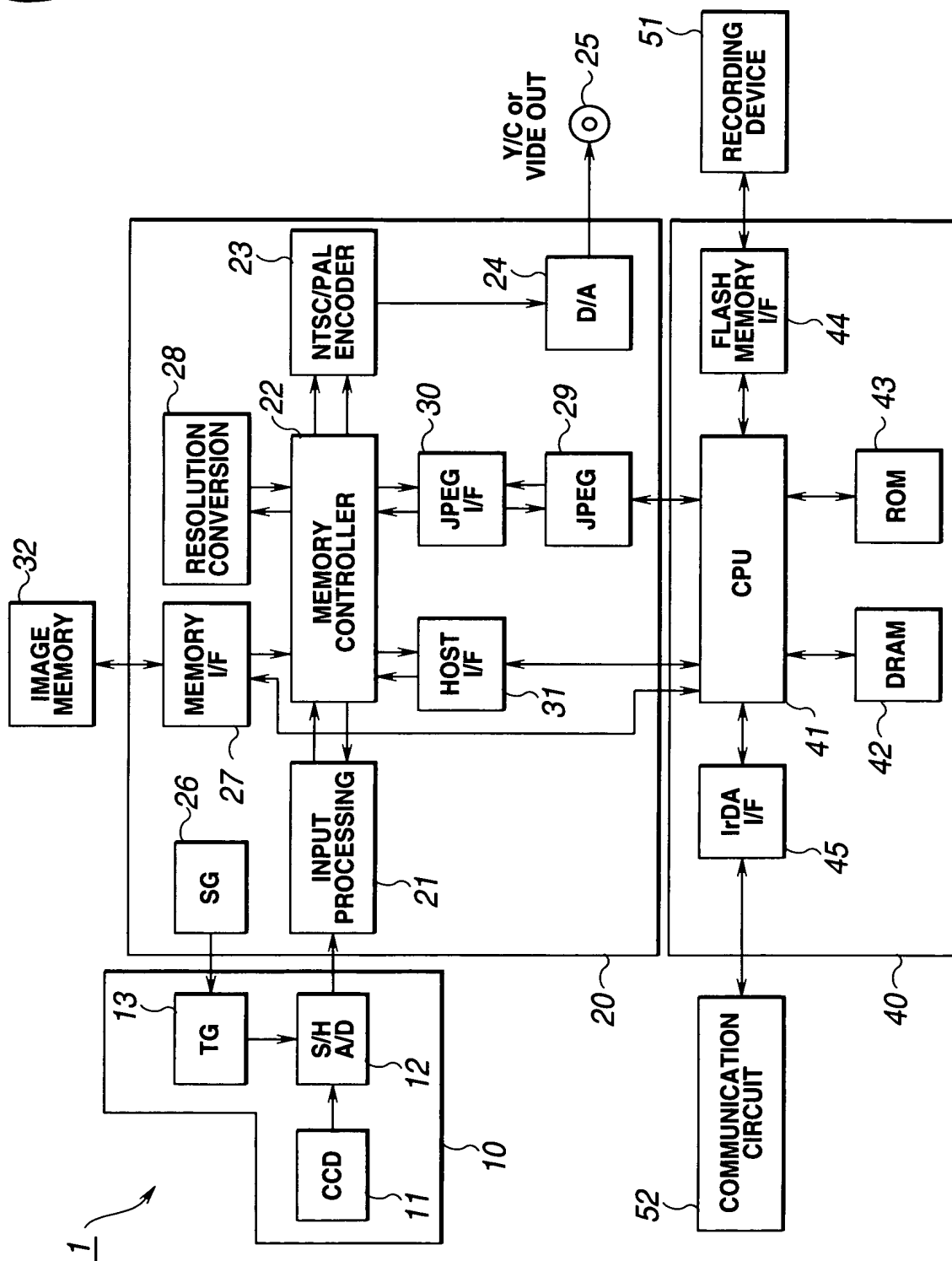


FIG.1

(PRIOR ART)



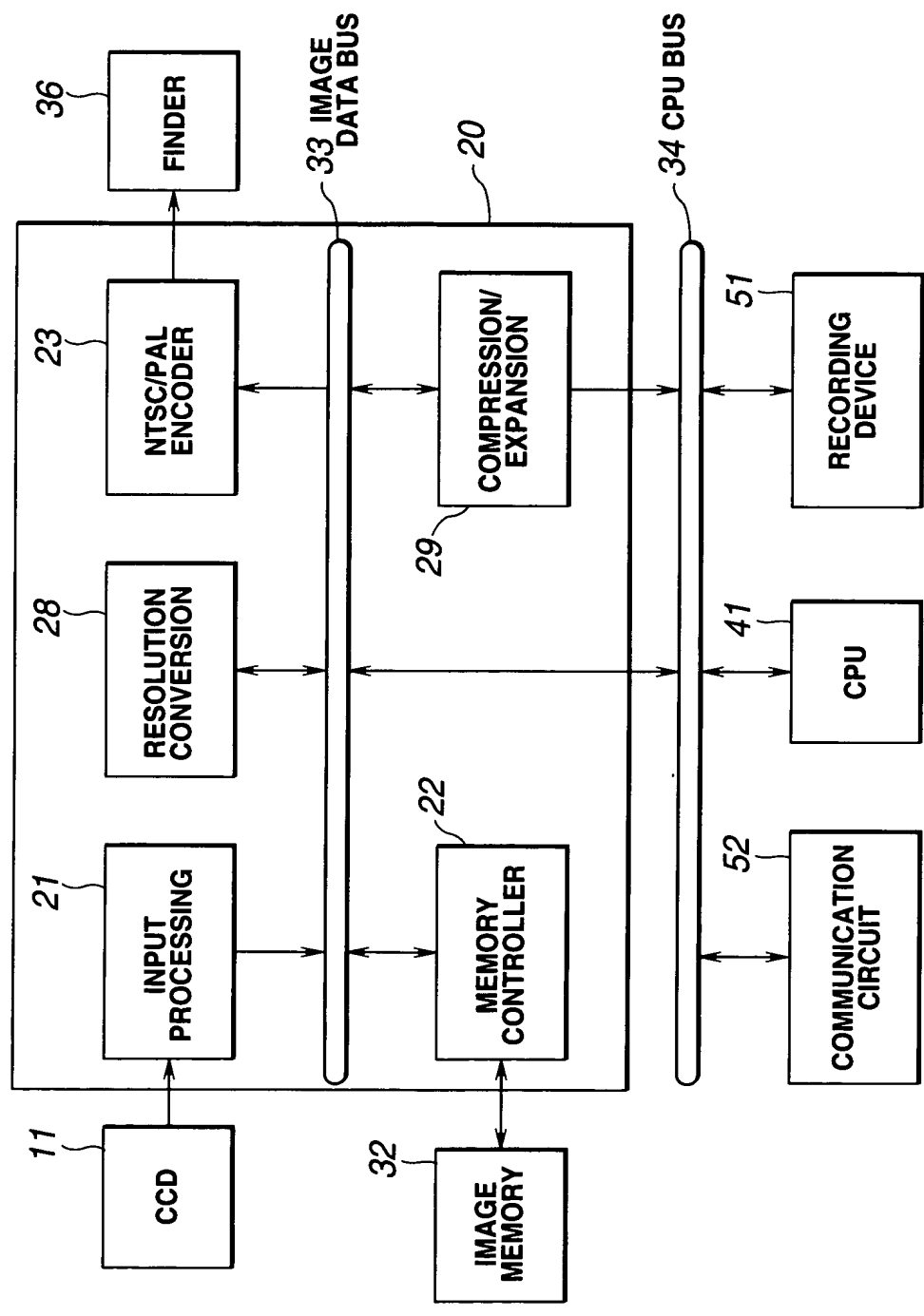


FIG.3



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Invention: Imaging Apparatus for ... Image Data
Serial No.: 09/354,476

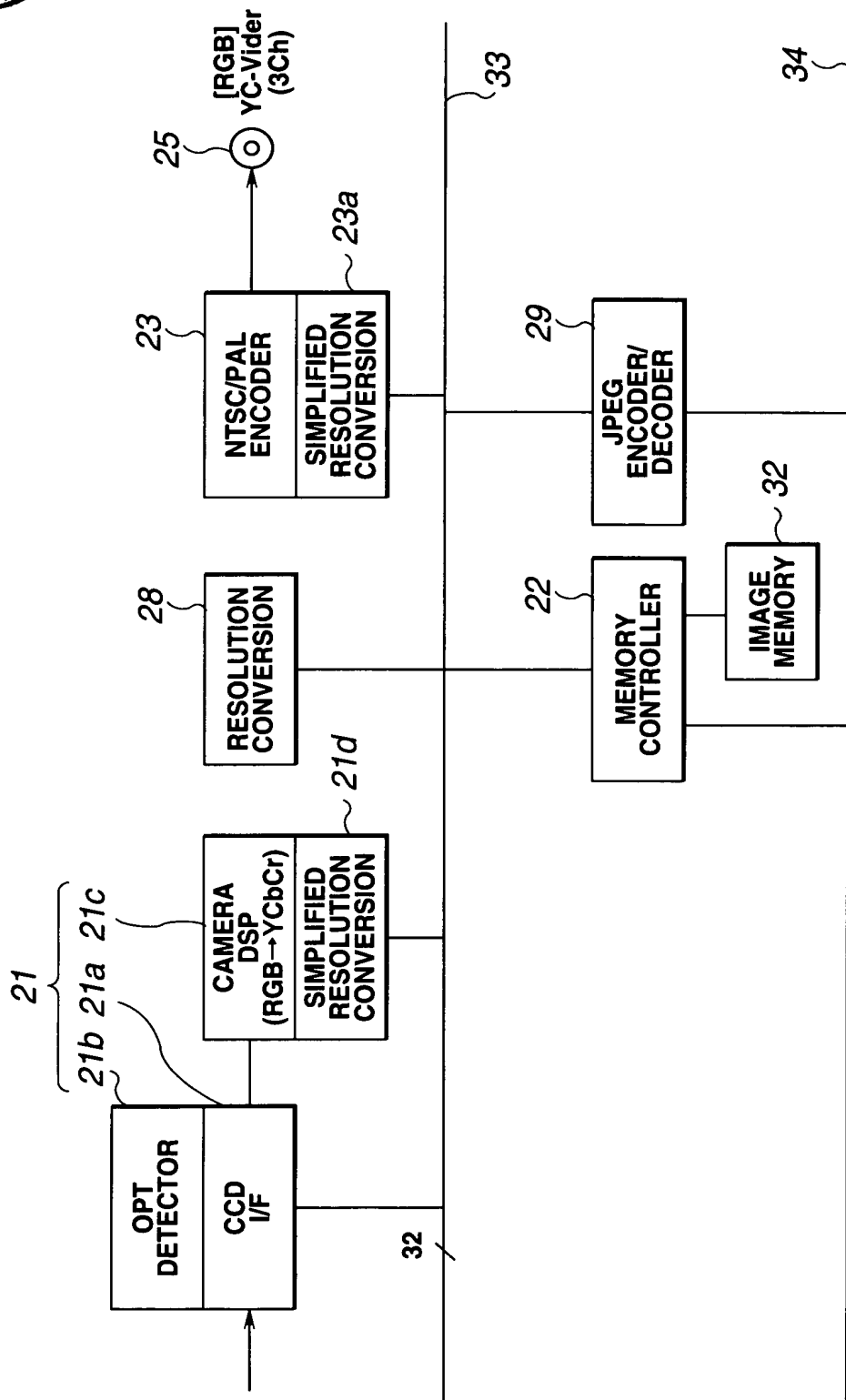


FIG.4

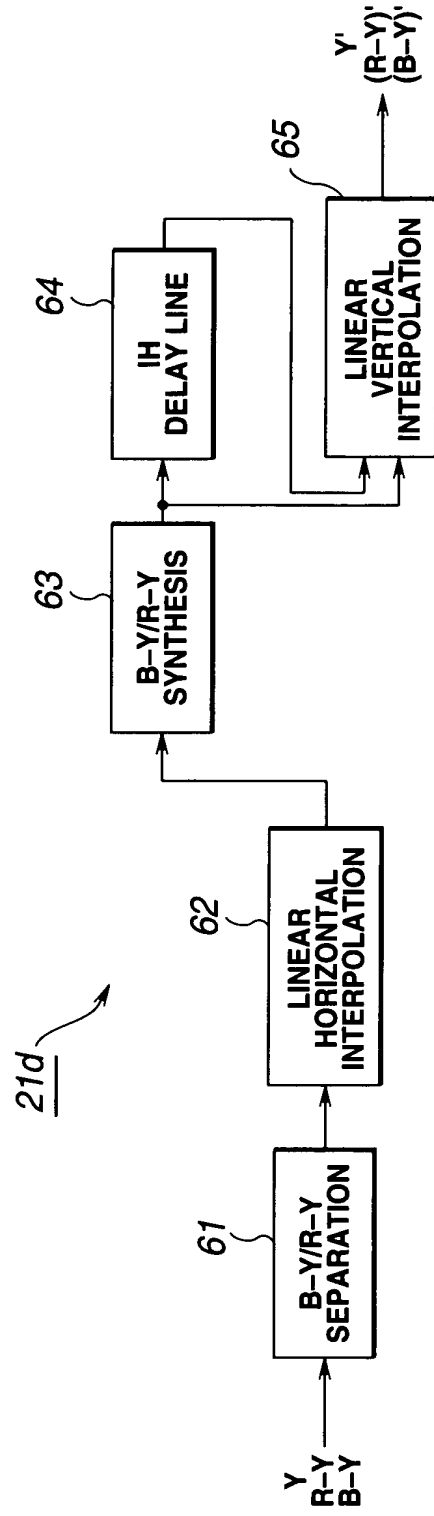


FIG.5

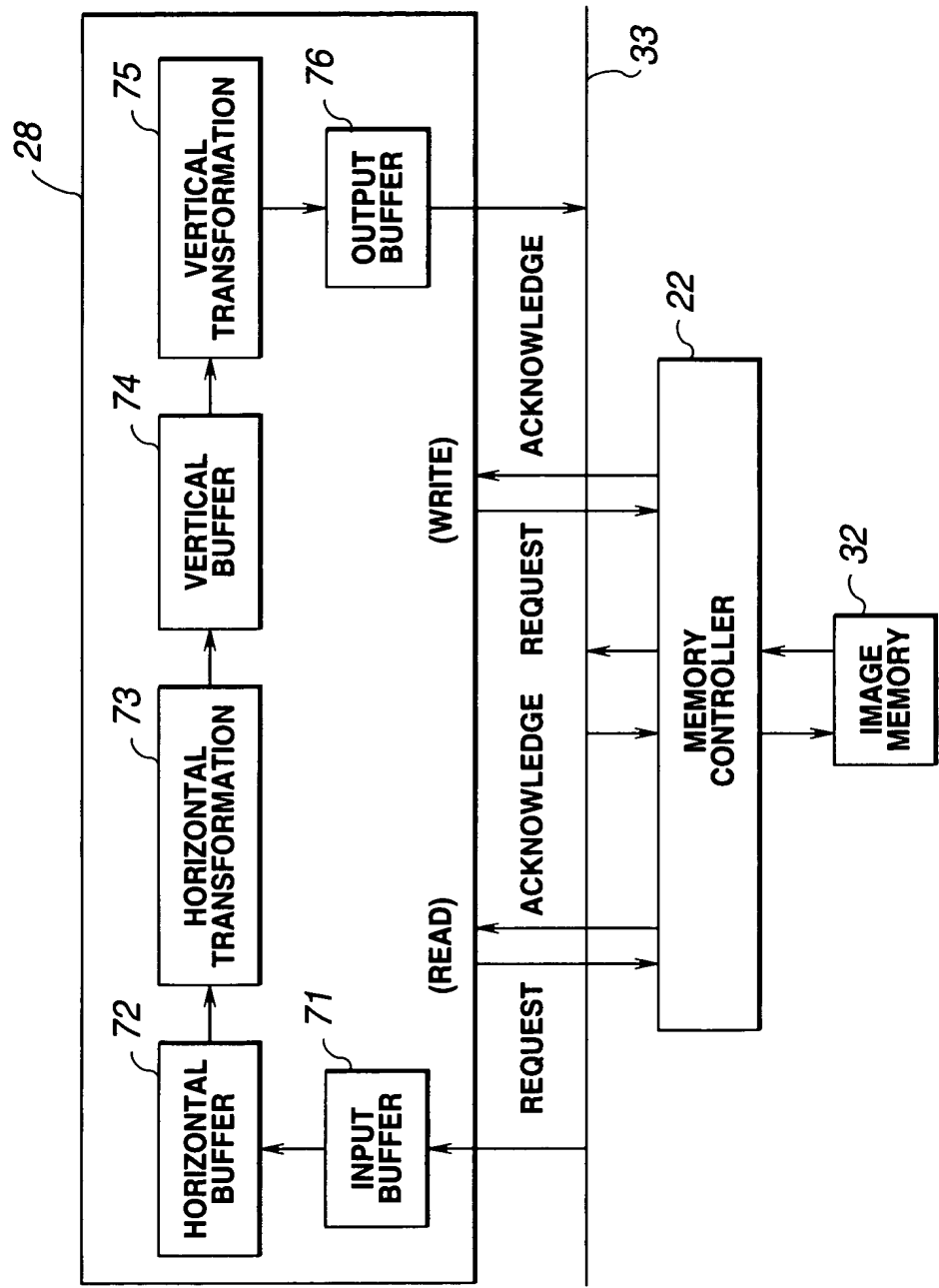


FIG.6

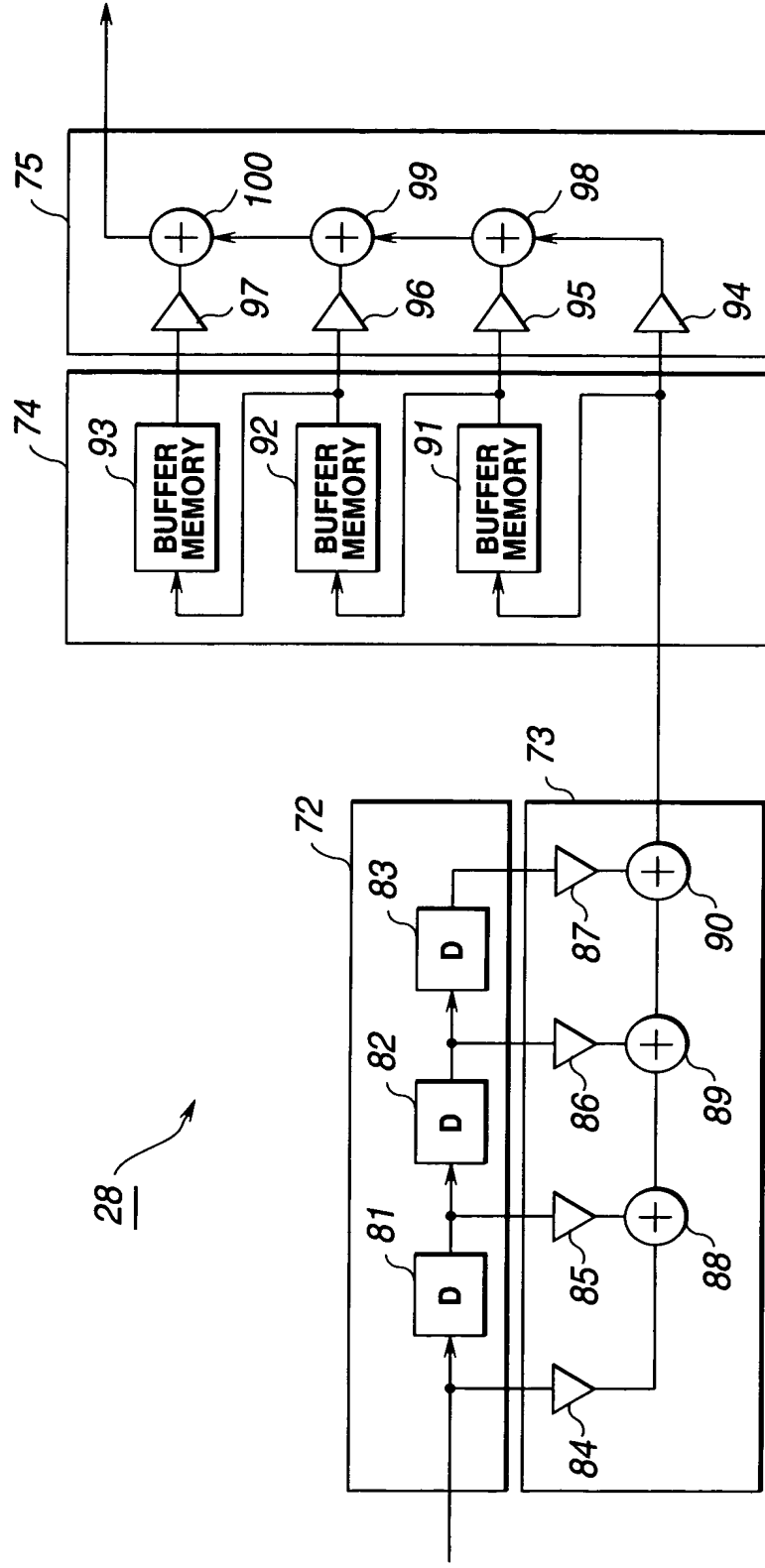


FIG.7

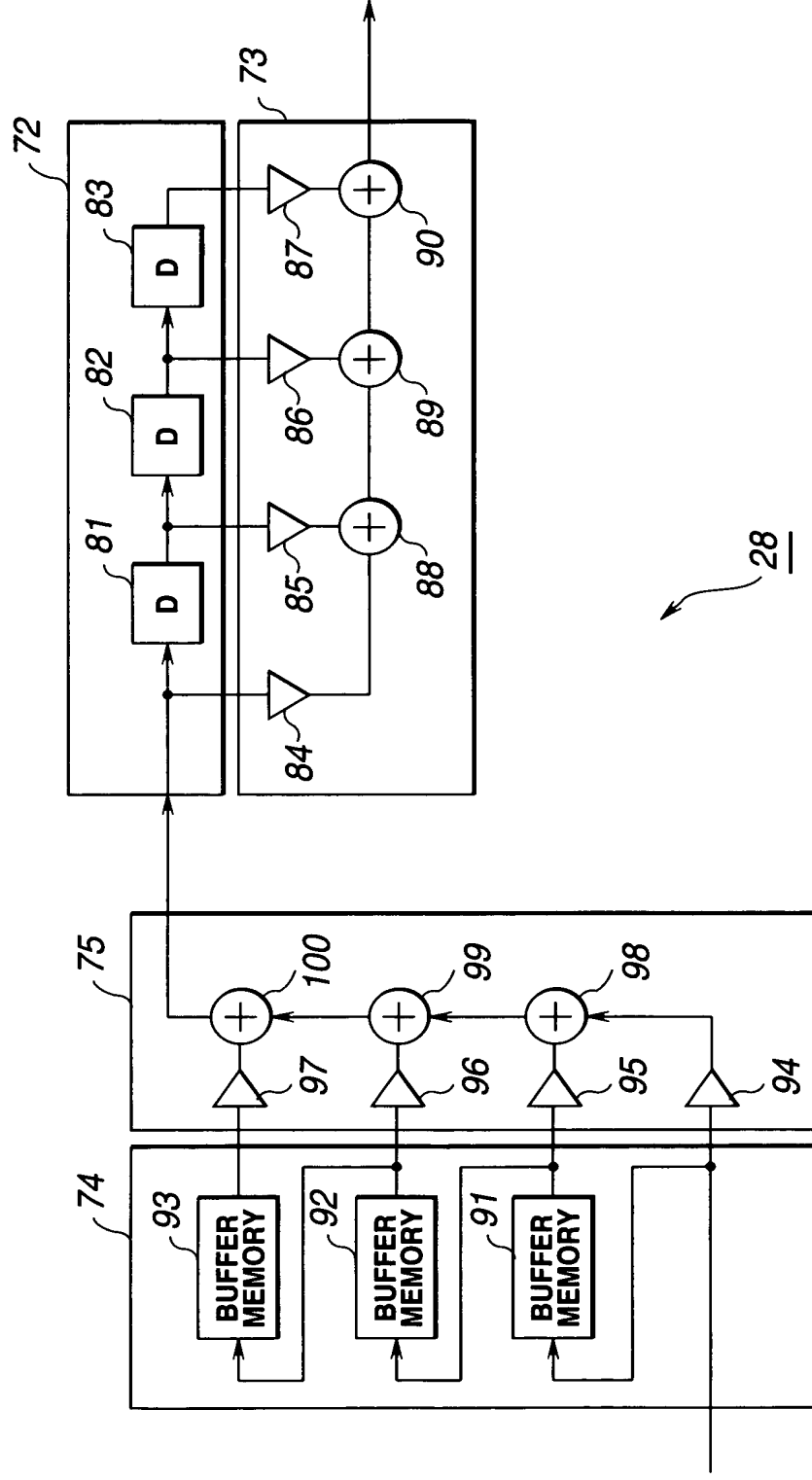


FIG.8



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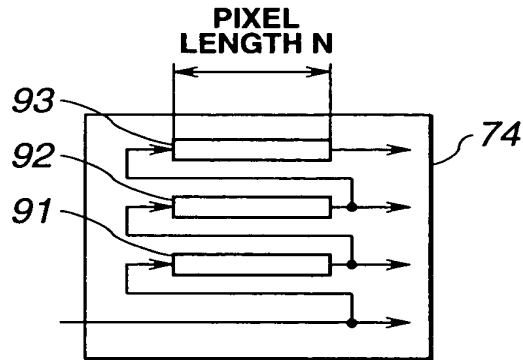


FIG. 9

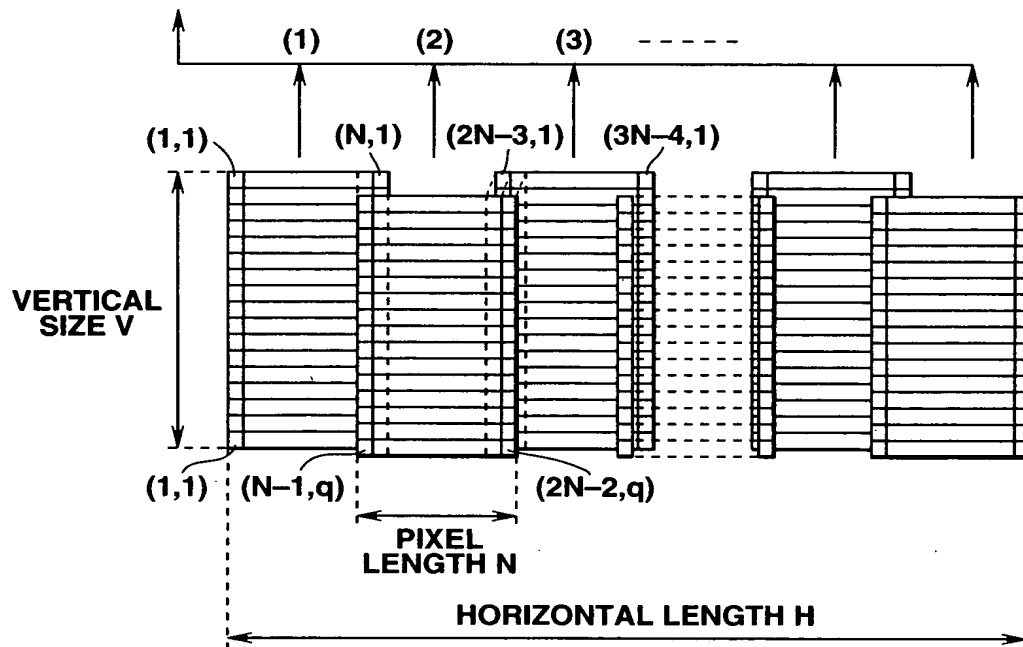


FIG. 10



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 Serial No.: 09/354,476

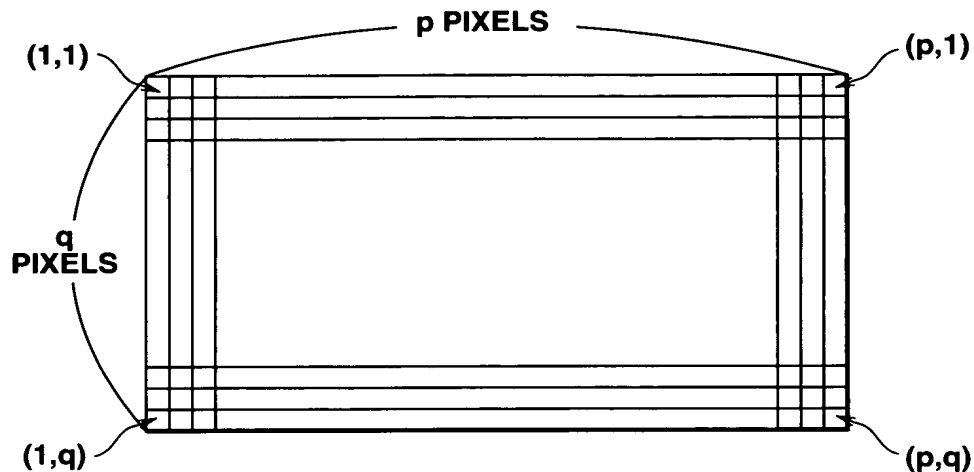


FIG.11

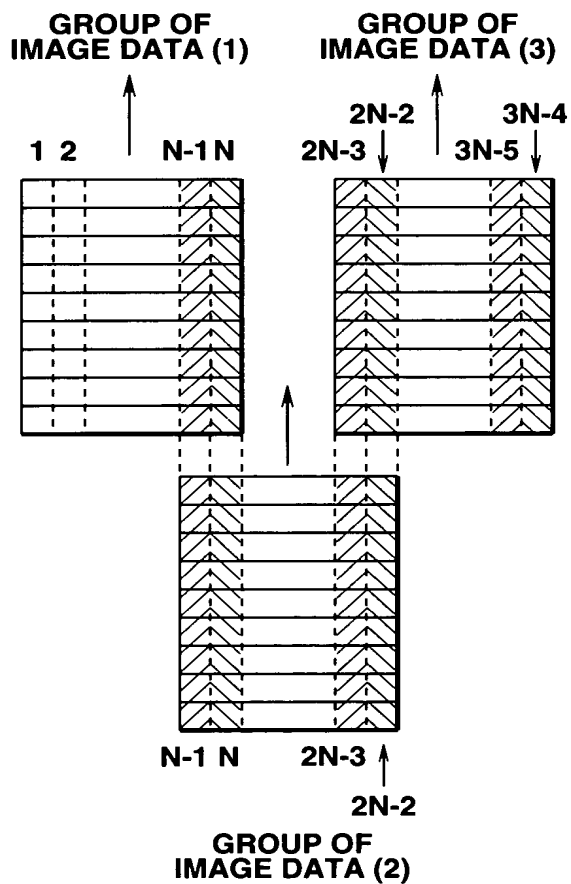


FIG.12



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Invention: Imaging Apparatus for ... Image Data
Serial No.: 09/354,476

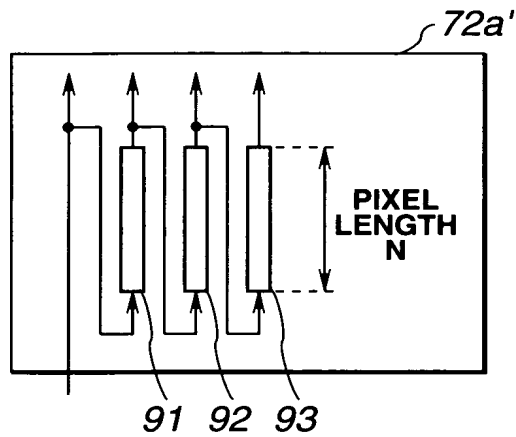


FIG.13

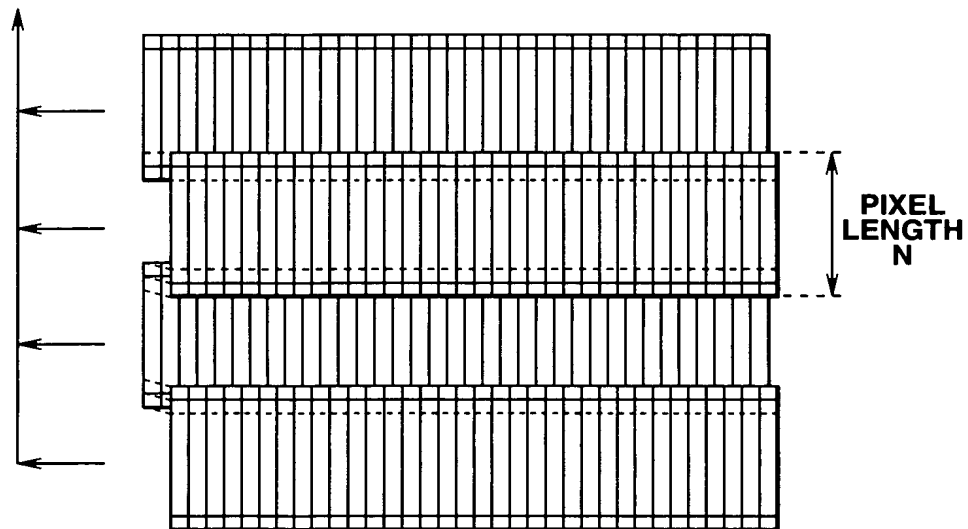


FIG.14



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Invention: Imaging Apparatus for ... Image Data
Serial No.: 09/354,476

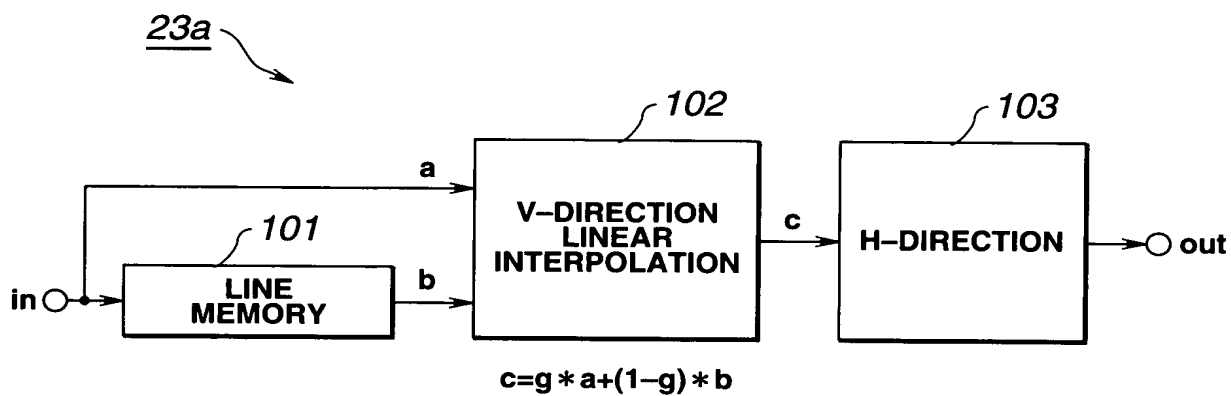


FIG.15

FIG. 16A ^{CCLK} 12.27MHz

FIG. 16B $\text{CCD1F} \rightarrow \text{CAMDSP}$

1/3 THINNING

FIG. 16C CAMDSP
→DRAM

FIG. 16D

	DRAM → NTSC								
Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Cb	Cr	Cb	Cr	Cb	Cr	Cb	Cr	Cb	Cr

[illegible]

FIG. 16F $\text{IBUS} \rightarrow \text{DRAM (16bit)}$

Diagram illustrating a data path for a 16-bit DRAM. The path starts with a **C → D** block, followed by a **D → N** block. The data then enters a large block divided into four sections: **D → N**, **C → D**, **D → O**, and **D → O**. Above this block, the label **DRAM → NTSC** is shown. The output of the large block is a **D → N** block, followed by a **D → N** block. Above these two blocks, the label **DRAM → OSD** is shown. The data then enters a **C → D** block, followed by a **D → N** block. Above these two blocks, the label **CAMDSP → DRAM** is shown. The final output is a **D → O** block.